REMARKS

Claims 1-46 are pending, with claims 1, 15, 23, 32 and 39 being independent. Claim 13 has been amended. No new matter has been added. Reconsideration and allowance of the above-referenced application are respectfully requested.

Claim 13 stands rejected under 35 U.S.C. 112, second paragraph, as allegedly being indefinite. Claim 13 has been amended to obviate the alleged lack of antecedent basis. Claim 1 recites, "a wakeup loop to hold scheduler instructions including unexecuted instructions, and to indicate ready instructions of the unexecuted instructions that may be ready to be executed". (Emphasis added.) Thus, there is clear antecedent basis for "the unexecuted, ready instructions" in claim 13. In view of this amendment, withdrawal of the rejection of claim 13 is respectfully requested.

Claims 1-4, 7, 10, 12-20, 23-26, 29, 32-34, 38-42 and 46 stand rejected under 35 U.S.C. 102(b) as allegedly being anticipated by Stark et al. (On Pipelining Dynamic Instruction Scheduling Logic). Claims 5-6, 8-9, 11, 21-22, 27-28, 30-31, 35-37 and 43-45 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Stark in view of Hennessy and

Patterson (Computer Architecture - A Quantitative Approach, 2nd Edition, 1996). These contention are respectfully traversed.

In the Response to Arguments section, the official action states, "applicant, in essence, claims that dependent instruction wakeup occurs before selection is confirmed for the instruction causing the wakeup." The official action then suggests that Stark anticipates this restatement of the claimed subject matter because, looking at Fig. 11 in Stark, the OR instruction causes the wakeup of the SUB instruction, and the OR instruction is confirmed as selected when the OR instruction is executed in cycle 3, which comes after the wakeup of the SUB instruction in cycle 2. But this line of reasoning overlooks the fact that the OR instruction is actually confirmed as selected prior to cycle 3, when its tag is broadcast in cycle 2.

Stark explicitly states this in section 4.4 during the description of Fig. 11b: "In cycle 2, the SUB wakes up after matching the tag broadcast by the OR." (Emphasis added.) This tag broadcast is in fact the confirmation of selection of the OR for execution, and the fact that the OR instruction is then subsequently executed in the next cycle is irrelevant. Stark's description of Fig. 11 makes clear that confirmation of selection of the OR instruction for execution occurs in the same cycle as the wakeup of the SUB instruction.

Additionally, the official action's restatement of the claimed subject matter is not the same as the actual language of the independent claims in this case. Independent claim 1 recites, "A processor comprising: a wakeup loop to hold scheduler instructions including unexecuted instructions, and to indicate ready instructions of the unexecuted instructions that may be ready to be executed; at least one of the unexecuted instructions to wakeup and notify at least another of the unexecuted instructions to speculatively wakeup before selection of the at least one of the unexecuted instructions is confirmed; and a select loop to select at least one of the ready instructions for execution." (Emphasis added.) The art of record fails to teach or suggest this claimed subject matter.

Independent claim 23 recites, "A system comprising: a random access memory device; and a processor in communication with the random access memory device, the processor including: a wakeup loop to hold scheduler instructions including unexecuted instructions, and to indicate ready instructions of the unexecuted instructions that may be ready to be executed; at least one of the unexecuted instructions to wakeup and notify at least another of the unexecuted instructions to speculatively wakeup before selection of the at least one of the unexecuted instructions is confirmed; and a select loop to select at least one of the ready instructions for execution." (Emphasis added.)

The art of record fails to teach or suggest this claimed subject matter.

Independent claim 32 recites, "A method of issuing requesting instructions to an execution unit, comprising: speculatively setting an indicator to indicate a requesting instruction is ready to be selected for execution, said speculatively setting being caused by a prior wakeup of an earlier instruction before selection of the earlier instruction is confirmed, the requesting instruction being a dependent of the earlier instruction; during a cycle, selecting a predetermined number of the requesting instructions having a set indicator; and resetting the indicator of the requesting instructions that are selected." (Emphasis added.) The art of record fails to teach or suggest this claimed subject matter.

Independent claim 39 recites, "A method of issuing unexecuted instructions to an execution unit, comprising: generating resource vectors corresponding to the unexecuted instructions, the resource vectors including resource indicators to indicate availability of resources; speculatively setting the resource indicators to indicate resources associated with corresponding ones of the unexecuted instructions are available so that the corresponding ones of the unexecuted instructions are ready to be executed, said speculatively setting being caused by a prior wakeup of one or more earlier instructions

before selection of the one or more earlier instruction is confirmed; and selecting a predetermined number of the corresponding ones of the unexecuted instructions." (Emphasis added.) The art of record fails to teach or suggest this claimed subject matter.

Independent claim 15 recites, "A processor comprising: a select-free scheduler including wakeup and select logic having a total scheduling latency, to schedule instructions for functional units that execute instructions having an execution latency that is less than the total scheduling latency of the wakeup and select logic." (Emphasis added.) The official action states that the term "select-free" is "merely a label". This is incorrect. The term "select-free" clearly defines specific structure of the scheduler within the context of the disclosure. This limitation of the claim must be found in the prior art in order for the claim to be anticipated.

The structure corresponding to this claim limitation is clearly articulated in the application as filed. The application makes clear that select-free scheduling logic breaks the scheduling loop "into two smaller loops: a loop for wakeup and a loop for select." (See the present specification at paragraph 13.) "With select-free scheduling logic, an instruction speculates that it will be selected for execution. The instruction asserts the AVAILABLE lines for its wakeup array

entries before selection of the instruction is confirmed." (See the present specification at paragraph 29.)

"Because there is usually no more than one instruction per wakeup array requesting execution, it is possible to speculate that any waking instruction will be selected for execution. Select-free scheduling logic exploits this fact by removing the select logic 102 from the critical scheduling loop and scheduling instructions speculatively. The select logic 102 is instead used to confirm that the schedule is correct. By breaking this loop, the processor cycle time is no longer set by the time required for wakeup and select, but is instead set just by the time required for wakeup." (See the present specification at paragraph 30.)

In view of the description and the figures of the present application, one skilled in the relevant art would clearly understand the processor structures described by the claim limitation "select-free scheduler". One skilled in the art would not believe that "select-free scheduler" means there is no selection logic at all in the instruction scheduler, as is suggested in the Response to Arguments section of the official action.

In view of the above remarks, independent claims 1, 15, 23, 32 and 39 should be in condition for allowance. Dependent

claims 2-14, 16-22, 24-31 and 40-46 are patentable based on the above arguments and their own merits.

It is respectfully suggested for all of these reasons, that the current rejection is totally overcome; that none of the cited art teaches or suggests the features which are claimed, and therefore that all of these claims should be in condition for allowance. A formal notice of allowance is thus respectfully requested.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific issue or comment does not signify agreement with or concession of that issue or comment. Because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

No fees are believed due with this response. Please apply any necessary charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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